AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) The apparatus according to claim 7 [[2]], wherein the N-channel isolation MOS transistor comprises an isolated NMOS transistor.

4. (Currently Amended) The apparatus according to claim 7 [[2]], wherein the N-channel MOS blocking transistor comprises an NMOS transistor.

5. (Currently Amended) The apparatus according to claim 7 [[2]], wherein the N-channel MOS blocking transistor comprises a Lateral double-diffused LDMOS transistor.

6. (Currently Amended) The apparatus according to claim 7 [[2]], wherein the N-channel MOS blocking transistor comprises a drain-extended DE NMOS transistor.

7. (Currently Amended) An apparatus comprising a reverse current blocking circuit devoid of PMOS, bipolar PNP, and external circuit protection devices, wherein the reverse current blocking circuit is operational to protect the apparatus against reverse current flow; wherein the reverse blocking circuit comprises:

an N-channel MOS isolation transistor; and

an N-channel MOS blocking transistor, wherein a reverse supply voltage connection operates to turn-on the N-channel MOS isolation transistor, and further wherein the turn-on of the N-channel MOS isolation transistor operates to turn-off the N-channel MOS blocking transistor to prevent the flow of reverse current there through in response to the reverse supply voltage connection;

~~The apparatus according to claim 2, further comprising:~~

a regulated voltage output node;

a voltage regulator output N-channel MOS transistor having its drain coupled to the drain of the N-channel MOS blocking transistor, and further having its source connected to the output node;

a bias generator operational to generate a bias current for the voltage regulator output N-channel MOS transistor; and

a regulator operational to control the gate of the voltage regulator output N-channel MOS transistor to hold the regulated voltage output node at a desired regulation point.

8. (Cancelled)

9. (Currently Amended) The apparatus according to claim 17 [[8]], wherein the reverse supply voltage connection protecting means is operational to protect the apparatus against reverse current flow in a high side current path connected to a supply voltage.

10. (Currently Amended) The apparatus according to claim 17 [[8]], wherein the reverse supply voltage connection protecting means is operational to protect the apparatus against reverse current flow in a low side current path connected to ground.

11. (Cancelled)

12. (Currently Amended) The apparatus according to claim 17 [[11]], wherein the reverse supply voltage connection protecting means comprises:

an N-channel MOS isolation transistor; and

an N-channel MOS current blocking transistor, wherein a reverse supply voltage connection operates to turn-on the N-channel MOS isolation transistor, and further wherein the turn-on of the N-channel MOS isolation transistor operates to turn-off the N-channel MOS current blocking transistor to prevent the flow of reverse current there through in response to the reverse supply voltage connection such that the means for passing a supply voltage to the regulated voltage output node below a desired regulation level is protected against the reverse supply connection.

13. (Original) The apparatus according to claim 12, wherein the N-channel isolation MOS transistor comprises an isolated NMOS transistor.

14. (Original) The apparatus according to claim 12, wherein the N-channel MOS blocking transistor comprises an NMOS transistor.

15. (Original) The apparatus according to claim 12, wherein the N-channel MOS blocking transistor comprises a Lateral double-diffused LDMOS transistor.

16. (Original) The apparatus according to claim 12, wherein the N-channel MOS blocking transistor comprises a drain-extended DE NMOS transistor.

17. An apparatus comprising means for protecting the apparatus against reverse supply voltage connections, wherein the reverse supply voltage connection protecting means is devoid of PMOS devices, bipolar PNP devices, and protection devices external to the apparatus;

a regulated voltage output node; and

means for passing a supply voltage to the regulated voltage output node below a desired regulation level;

~~The apparatus according to claim 11,~~ wherein the means for passing a supply voltage to the regulated voltage output node below a desired regulation level comprises:

a voltage regulator output N-channel MOS transistor having its drain coupled to the drain of the N-channel MOS blocking transistor, and further having its source connected to the output node;

a bias generator operational to generate a bias current for the voltage regulator output N-channel MOS transistor; and

a regulator operational to control the gate of the voltage regulator output N-channel MOS transistor to hold the regulated voltage output node at a desired regulation point.

18. (Cancelled)

19. (Cancelled)

20. (Currently Amended) An apparatus operational to pass a supply voltage to an output node below a desired regulation level, wherein the apparatus is protected against a reverse supply connection without use of PMOS, bipolar PNP, or external pre-regulator protection devices comprising:

a N-channel MOS isolation transistor; and

a N-channel MOS current blocking transistor, wherein a reverse supply voltage connection operates to turn-on the N-channel MOS isolation transistor, and further wherein the turn-on of the N-channel MOS isolation transistor operates to turn-off the N-channel MOS current blocking transistor to prevent the flow of reverse current there through in response to the reverse supply voltage connection such that the apparatus is protected against the reverse supply connection; and

~~The apparatus according to claim 19, further comprising:~~

a voltage regulation circuit comprising:

a voltage regulator output N-channel MOS transistor having its drain coupled to the drain of the N-channel MOS current blocking transistor, and further having its source connected to the output node;

a bias generator operational to generate a bias current for the voltage regulator output N-channel MOS transistor; and

a regulator operational to control the gate of the voltage regulator output N-channel MOS transistor to hold the regulated voltage output node at a desired regulation point.

21. (Cancelled)